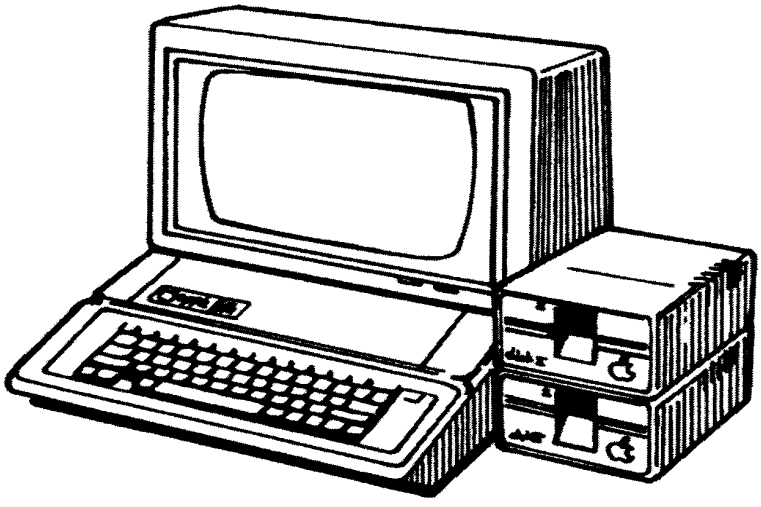
Apple ][ Computer Information

# IWM Floppy Disk I/O Controller Info

# 6502 assembly program to determine if IWM or Disk ][ disk state machine is installed

Apple Computer, Inc. -- January 1984



SOURCE
Brutal Deluxe Software web site -- www.brutal-deluxe.fr
31 December 2008

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OURCE   FILE #01 =>IWM
000:                1 *
000:                2 *
000:                3 * THIS ROUTINE WILL DETERMINE WHETHER A STATE MACHINE DISK II CONTROLLER
000:                4 * OR AN IWM CONTROLLER IS INSTALLED IN THE SYSTEM.
000:                5 * UPON EXIT FROM THE ROUTINE, Y=1 MEANS IWM CONTROLLER AND Y=0 MEANS
000:                6 * STATE MACHINE DISK II CONTROLLER.
000:                7 *
000:                8 * ASSUME A MOTOR OFF INSTRUCTION [LDA $C088,X] HAS BEEN EXECUTED FOR
000:                9 * TWO SECONDS BEFORE THE USER CALLS ON THIS ROUTINE.  OTHERWISE, A
000:               10 * TWO SECOND DELAY LOOP MUST BE ADDED AFTER THE FIRST MOTOR OFF
000:               11 * INSTRUCTION [LDA $C088,X]  AT THE BEGINNING OF THIS ROUTINE.
000:               12 *
000:               13 * THE ENABLED DISK DRIVE WILL CONTINUE TO BE ON FOR 1 SEC
000:               14 * AFTER EXIT FROM THIS ROUTINE.
000:               15 *
000:               16 *
---- NEXT OBJECT FILE NAME IS IWM.0
000:        1000   17            ORG   $1000
000:AE 41 10       18            LDX   SLOTX16       ;X REG=SLOT NO. X 16
003:BD 88 C0       19            LDA   $C088,X       ;MOTOR OFF
006:A0 00          20            LDY   #00           ;CLEAR REG. Y
008:BD 8D C0       21            LDA   $C08D,X       ;Q6H
00B:BD 8F C0       22            LDA   $C08F,X       ;Q7H, ADDRESS MODE REG.
00E:A9 04          23            LDA   #$04
010:9D 8F C0       24            STA   $C08F,X       ;DISABLE TIMER BIT IN MODE REG.
013:BD 8E C0       25            LDA   $C08E,X       ;Q7L, OUT OF WRITE MODE
016:BD 89 C0       26            LDA   $C089,X       ;MOTOR ON
019:48             27 LOOP       PHA                  ;10 MSEC DELAY LOOP
01A:68             28            PLA                  ;WAIT FOR THE MOTOR ON
01B:48             29            PHA                  ;SIGNAL TO BE ACTIVE IN
01C:68             30            PLA                  ;THE CONTROLLER CARD
01D:48             31            PHA
01E:68             32            PLA
01F:48             33            PHA
020:68             34            PLA
021:48             35            PHA
022:68             36            PLA
023:C8             37            INY
024:D0 F3   1019   38            BNE   LOOP          ;END OF DELAY LOOP
026:BD 8E C0       39            LDA   $C08E,X       ;Q7L, READ STATUS REG.
029:9D 88 C0       40            STA   $C088,X       ;MOTOR OFF
02C:29 1F          41            AND   #$1F          ;MASK 5 L.S. BITS
02E:C9 04          42            CMP   #$04          ;CHECK TIMER BIT
030:D0 09   103B   43            BNE   DISKII        ;DISK II CONTROLLER IF NOT EQ
032:C8             44 IWM        INY                  ;INCREMENT Y REG.
033:BD 8F C0       45            LDA   $C08F,X       ;Q7H, ADDRESS MODE REG.
036:A9 00          46            LDA   #$00
038:9D 8F C0       47            STA   $C08F,X       ;Q7H, RESTORE MODE REG.
03B:BD 8E C0       48 DISKII     LDA   $C08E,X       ;Q7L,
03E:BD 8C C0       49            LDA   $C08C,X       ;Q6L, RESTORE TO READ MODE
041:        1041   50 FIN        EQU   *
041:60             51 SLOTX16    DFB   $60
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;03B DISKII          ?1041 FIN           ?1032 IWM           1019 LOOP
1041 SLOTX16
* SUCCESSFUL ASSEMBLY := NO ERRORS
* ASSEMBLER CREATED ON 15-JAN-84 21:28
* TOTAL LINES ASSEMBLED    51
* FREE SPACE PAGE COUNT    89
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