

A<sub>3</sub> A<sub>2</sub> A<sub>1</sub> A<sub>0</sub>

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0/1	000D	Phase 0	
2/3	001D	Phase 1	
4/5	010D	Phase 2	
6/7	011D	Phase 3	
8/9	100D	Motor On	Enable whatever drive selected
A/B	101D	Drv Sel	
C/D	110D	Q6	
E/F	111D	Q7	

Q7	Q6	Motor On	Register Selected
0	0	0	Read all ones
0	0	1	Read Data
0	1	X	Read Status
1	0	X	Read Write - HSHK
1	1	0	Set Mode
1	1	1	WRITE DATA

~~Reading a register requires Q6 = Q7 = 10 or Motor On~~  
 IF MOTOR ON, Q6 = Q7 = HI to read  
 IF MOTOR OFF, Q6 = Q7 = LO to read

CAΦ = PHΦ  
 1 = PH1  
 2 = PH2  
 SEL = HDSEL

NBCD Dn	6	6	7	030
TAS Dn	16	16	19	020
TAS (AN)	14	14	16	020
ASL Dn	5	8	10	

FMT BYTE has INTLV  
 sets = double sided



Speeddrive: Timing diagrams indicate RDY lies about status for 150µS after issuing step. Thus seek should delay 150µS before checking for "seek done"

READY: If not up to speed, RDY always false. Can do RETAL by using  $\text{TRK}\phi$  sensor to know it's done.

Must know you <sup>were</sup> ready before <sup>post-</sup> seek routine spins on ready.

First Motor-on must be 500 mSec. This is first after ~~motor~~ insertion. Must stay on for 500 mSec.

Max RDY after Motor-on is 600 mSec  
No MIN spec.

Changing MFM  $\leftrightarrow$  GCR can take as long as a motor-on.

JWM SWITCHES

C0N0	—	RESET PH0
C0N1	—	SET PH0
C0N2	—	RESET PH1
C0N3	—	SET PH1
C0N4	—	RESET PH2
C0N5	—	SET PH2
C0N6	—	RESET PH3
C0N7	—	SET PH3
C0N8	—	MOTOR OFF
C0N9	—	MOTOR ON
C0NA	—	RESET LSTRB (DR1 SEL)
C0NB	—	SET LSTRB (DR2 SEL)
C0NC	—	RESET L6
C0ND	—	SET L6
C0NE	—	RESET L7
C0NF	—	SET L7

L7      L6      MOTOR ON

0	0	0
0	0	1
0	0	X
0	0	X
0	0	X
0	0	0
0	0	0

READ ALL ONES  
 READ DATA REG.  
 READ STATUS  
 READ WRITE-NANISHAKE  
 WRITE MODE REG.  
 WRITE DATA REG.